μPD27C1024A
65,536 x 16-Bit
CMOS UV EPROM

Description

The μPD27C1024A is a 1,048,576-bit ultraviolet erasable and electrically programmable ROM fabricated with an advanced CMOS process for substantial power savings. The device is organized as 65,536 words by 16 bits and operates from a single + 5-volt power supply. All inputs and outputs are TTL-compatible.

The μPD27C1024A is available in a 40-pin ceramic DIP with quartz window.

Features

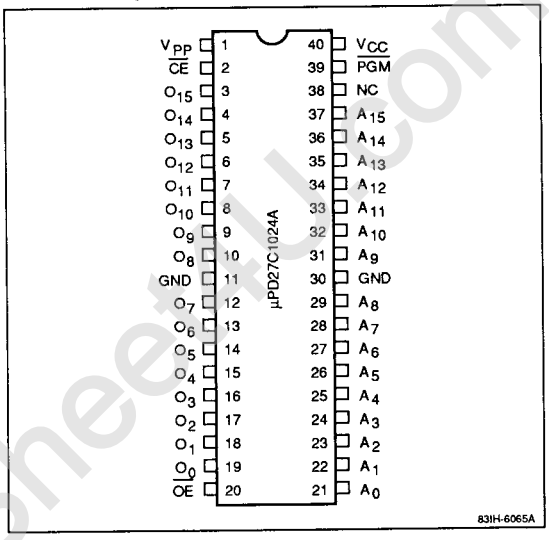
- 65,536 x 16-bit organization
- Ultraviolet erasable and electrically programmable
- High-speed word and page programming
- Low power dissipation
  - — 50 mA max (active)
  - — 100 μA max (standby)
- TTL-compatible inputs and outputs
- Three-state outputs
- Single + 5-volt power supply
- Advanced CMOS technology
- 40-pin cerdip packaging with quartz window

Ordering Information

Part Number	Access Time (max)	Package
μPD27C1024AD-12	120 ns	40-pin cerdip with quartz window
D-15	150 ns	
D-20	200 ns	

Pin Configuration

40-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
O_0 - O_{15}	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Program
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage
NC	No connection

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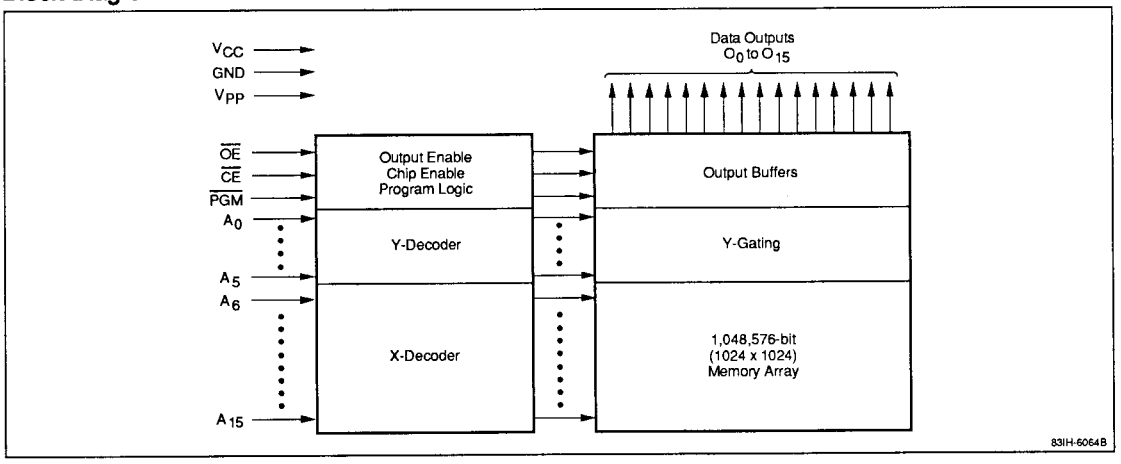
Block Diagram



Absolute Maximum Ratings

Operating temperature, T_{OPR}	−10 to +80°C
Storage temperature, T_{STG}	−65 to +125°C
Output voltage, V_{OUT}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to V_{CC} + 0.3 V
Input voltage, A_9	−0.6 to +13.5 V
Supply voltage, V_{CC}	−0.6 to +7.0 V
Supply voltage, V_{PP}	−0.6 to +13.5 V

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			14	pF
Output capacitance	C_{OUT}			16	pF

Truth Table

Function	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	5.0 V	5.0 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	5.0 V	5.0 V	High-Z
Standby	V_{IH}	X	X	5.0 V	5.0 V	High-Z
Page data latch	V_{IH}	V_{IL}	V_{IH}	12.5 V	6.5 V	D_{IN}
Page program	V_{IH}	V_{IH}	V_{IL}	12.5 V	6.5 V	High-Z
Word program	V_{IL}	V_{IH}	V_{IL}	12.5 V	6.5 V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	12.5 V	6.5 V	D_{OUT}
Program inhibit	X	V_{IL}	V_{IL}	12.5 V	6.5 V	High-Z
	X	V_{IH}	V_{IH}			

Notes:

(1) X = V_{IL} or V_{IH}.

(2) In read operation, $\overline{PGM}$ must be set to V_{IH} at all times, or for at least 2 μs before $\overline{OE}$ or $\overline{CE}$ returns to V_{IH}.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Read Operation or Standby					
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{PP}	V_{CC} – 0.6	V_{CC}	V_{CC} + 0.6	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–0.3		0.8	V
Operating temperature	T_A	0		70	°C
Programming Operation					
Supply voltage	V_{CC}	6.25	6.5	6.75	V
	V_{PP}	12.2	12.5	12.8	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	–0.3		0.8	V
Operating temperature	T_A	20	25	30	°C

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%; V_{PP} = V_{CC} ± 0.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read Operation						
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = –400 μA
	V_{OH2}	V_{CC} – 0.7			V	I_{OH} = –100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}	–10		10	μA	V_{OUT} = 0 to V_{CC}; $\overline{OE}$ = V_{IH}
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = 0 to V_{CC}
V_{PP} current	I_{PP}		1	100	μA	V_{PP} = V_{CC}
V_{CC} current (active)	I_{CCA1}			15	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			50	mA	f = 8.4 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH} min
	I_{CCS2}		1	100	μA	$\overline{CE}$ ≥ V_{CC} – 0.2 V; V_{IN} = 0 to V_{CC}

DC Characteristics (cont)

T_A = 25 ± 5°C; V_{CC} = +6.5 V ± 0.25; V_{PP} = +12.5 V ± 0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Programming Operation						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = 0 to V_{CC}
V_{PP} current	I_{PP}			50	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
V_{CC} current	I_{CC}			30	mA	

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%; V_{PP} = V_{CC} ± 0.6 V

Parameter	Symbol	μPD27C1024A-12 Min	μPD27C1024A-12 Max	μPD27C1024A-15 Min	μPD27C1024A-15 Max	μPD27C1024A-20 Min	μPD27C1024A-20 Max	Unit	Test Conditions
Read Operation									
Address to output delay	t_{ACC}		120		150		200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		120		150		200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}		60		70		70	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	50	0	55	0	55	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

AC Characteristics (cont)

T_A = 25 ± 5°C; V_{CC} = +6.5 V ± 0.25; V_{PP} = +12.5 V ± 0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Page Programming Operation						
Address setup time	t_{AS}	2			μs	
$\overline{CE}$ setup time	t_{CES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
	t_{AHL}	2			μs	
	t_{AHV}	0			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{OE}$ setup time	t_{OES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	
$\overline{OE}$ pulse width during data latch	t_{LW}	1			μs	
$\overline{PGM}$ setup time	t_{PGMS}	2			μs	
$\overline{CE}$ hold time	t_{CEH}	2			μs	
OE hold time	t_{OEH}	2			μs	

AC Characteristics (cont)

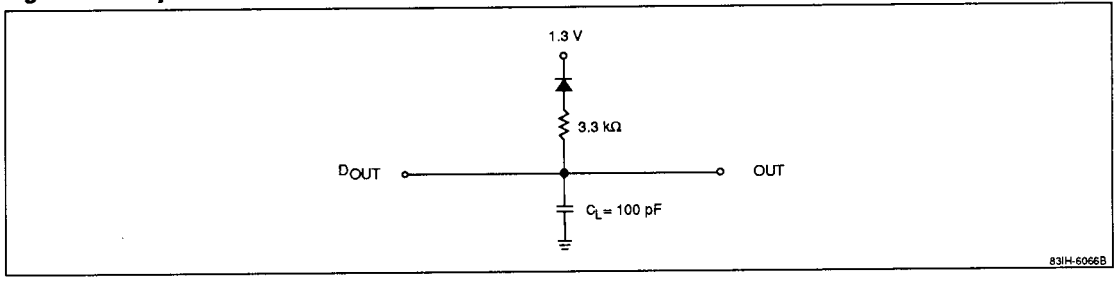
T_A = 25 ± 5°C; V_{CC} = +6.5 V ± 0.25; V_{PP} = +12.5 V ± 0.3

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Word Programming Operation						
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{CE}$ setup time	t_{CES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	

Notes:

(1) Input pulse levels = 0.45 to 2.4 V; input and output timing reference levels = 0.8 and 2.0 V; input rise and fall times ≤ 20 ns. See figure 1 for output load.

Figure 1. Output Load



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PROGRAMMING

Before programming the μPD27C1024A, erase all data; this sets all data bits high. The μPD27C1024A is originally shipped in this condition. To begin programming, first raise V_{CC} to +6.5 V ± 0.25, and then raise V_{PP} to 12.5 V ± 0.3. At this point, data to be programmed can be directly input in 16-bit format through the data bus. Programming causes relevant bits to go low.

Word Programming

For word programming, $\overline{CE}$ should be set low and $\overline{OE}$ high to start programming at the initial address. A 0.1-ms pulse is applied to $\overline{PGM}$, as shown in the word programming portion of the timing waveforms, and $\overline{OE}$ goes low to verify the 16 bits prior to making a program/no program decision. If the word is not programmed, another 0.1-ms pulse is applied to $\overline{PGM}$, up to a maximum of 10 times, before the next address is input. If the bits are not programmed in 10 tries, reject the device as a program failure.

After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ± 10% and verify all data again.

Page Programming

To begin page programming, $\overline{CE}$ and $\overline{PGM}$ should be set high and $\overline{OE}$ pulsed low twice to latch the addressed two-word, one-page data. $\overline{CE}$ and $\overline{OE}$ subsequently go high and a 0.1-ms program pulse is applied to $\overline{PGM}$, as shown in the page programming portion of the timing waveforms. Immediately thereafter, $\overline{CE}$ and $\overline{OE}$ go low to verify the data prior to a program/no program decision being made. If the two words of page data are not programmed, another 0.1-ms pulse is applied to $\overline{PGM}$, up to a maximum of 10 times. If the page is not programmed in 10 tries, reject the device as a program failure.

Program Inhibit

The program inhibit option can be used in either word or page operation to program one of multiple μPD27C1024A devices whose $\overline{CE}$ pins are independent and $\overline{OE}$, V_{PP}, and O_0 through O_{15} pins are connected in parallel. For word programming, $\overline{OE}$ must be high and $\overline{CE}$ of the device to be programmed low. For page programming, both $\overline{OE}$ and $\overline{CE}$ must be high. Applying a low-level TTL pulse to $\overline{PGM}$ of the device to be programmed and a high-level TTL pulse to the $\overline{PGM}$ pins of the other devices enables the one device to be programmed while the others are inhibited.

Program Verification

To verify that the device is correctly programmed, execute a normal read cycle with a high logic level applied to the $\overline{PGM}$ pin and a low logic level applied to the $\overline{CE}$ and $\overline{OE}$ pins of the device to be verified. A high should be applied to the $\overline{CE}$ or $\overline{OE}$ pin of all other devices.

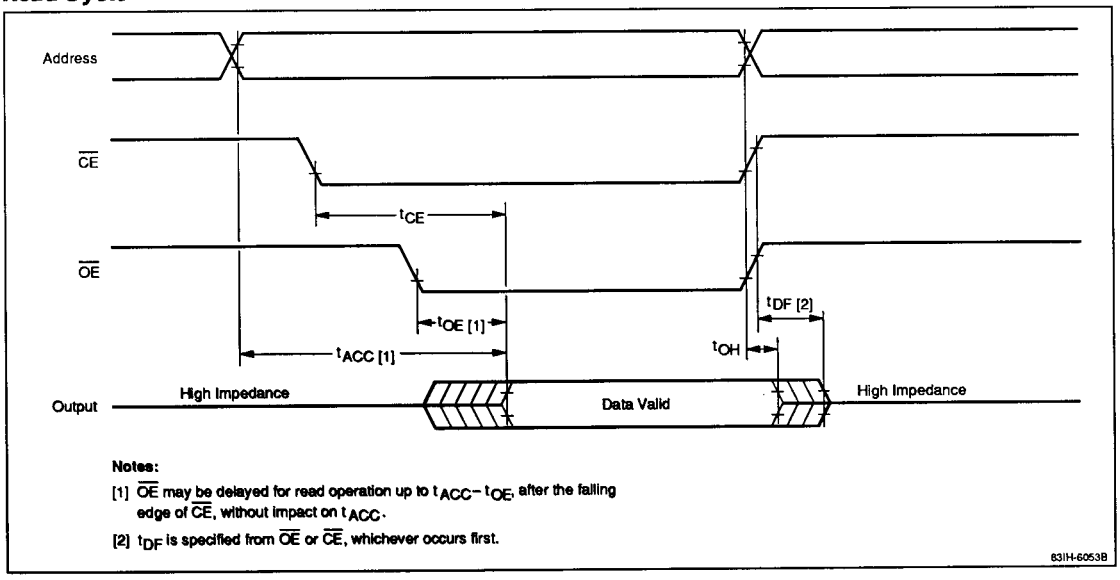
Erasure

Erase data on the μPD27C1024A by exposing it to light with a wavelength shorter than 400 nm. Since exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm^2 (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data. Using an ultraviolet lamp rated at 12,000 μW/cm^2, it takes approximately 20 minutes to complete erasure. Place the μPD27C1024A within 2.5 cm of the lamp tubes and remove any filter on the lamp.

Timing Waveforms

Read Cycle



Notes:

[1] $\overline{OE}$ may be delayed for read operation up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$, without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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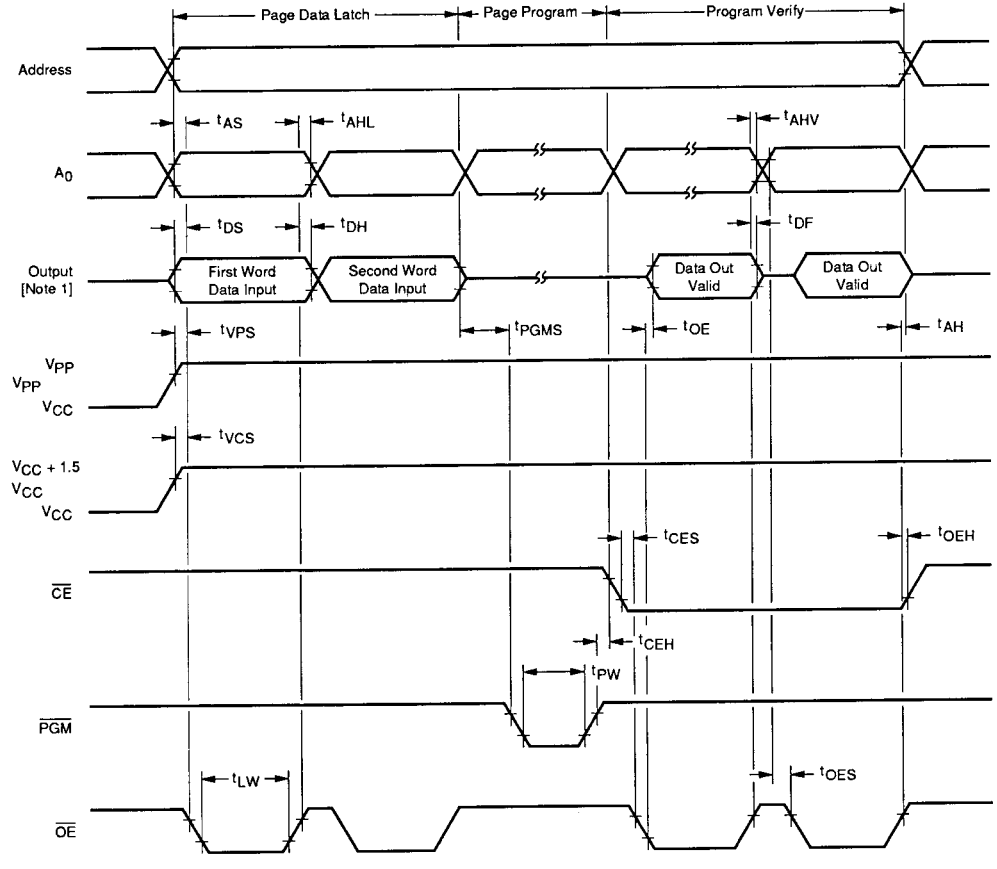
Timing Waveforms (cont)

Page Programming Cycle



Notes:

[1] The output lines are also used for data input when programming the device.

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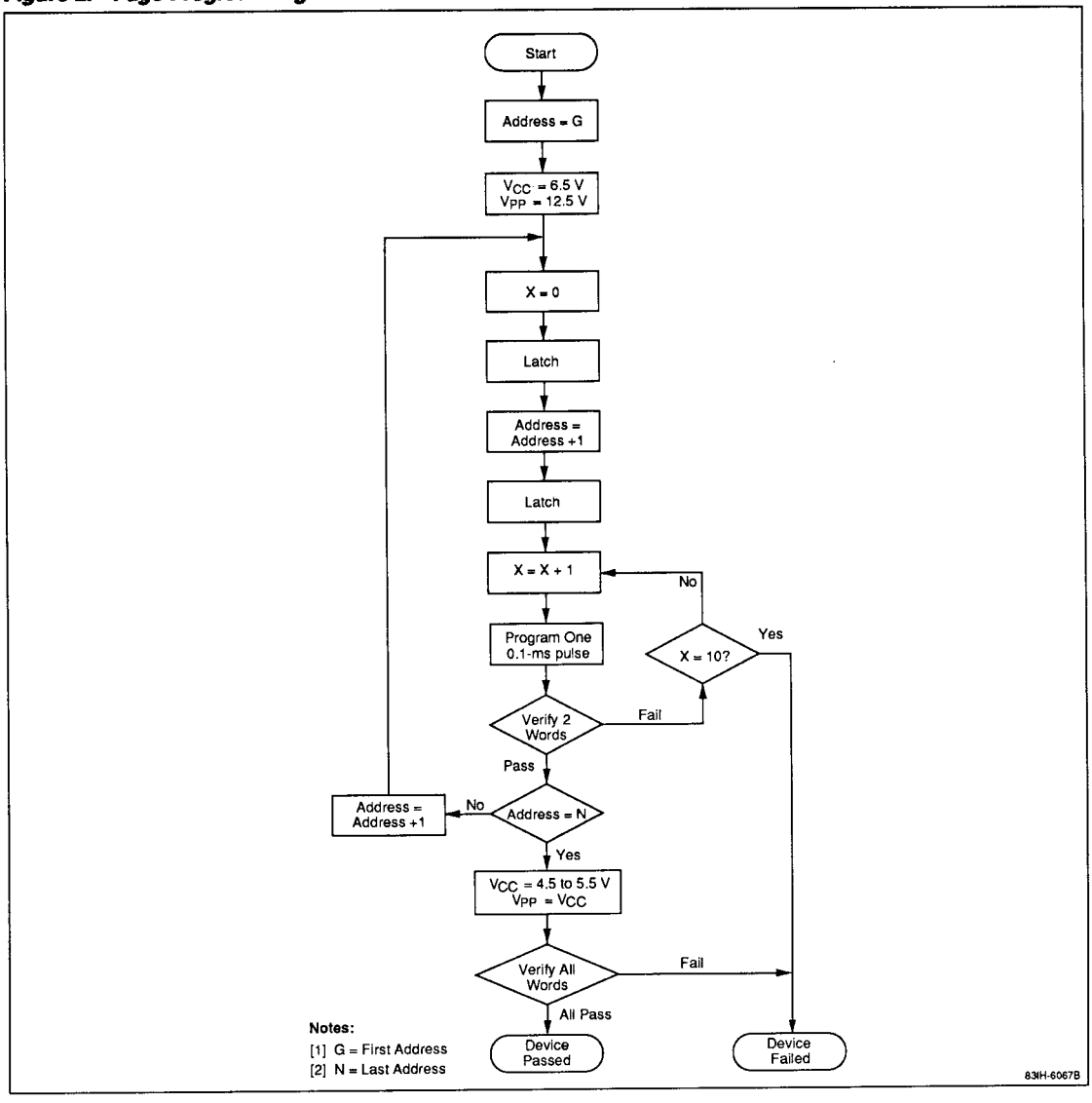
Figure 2. Page Programming Flowchart



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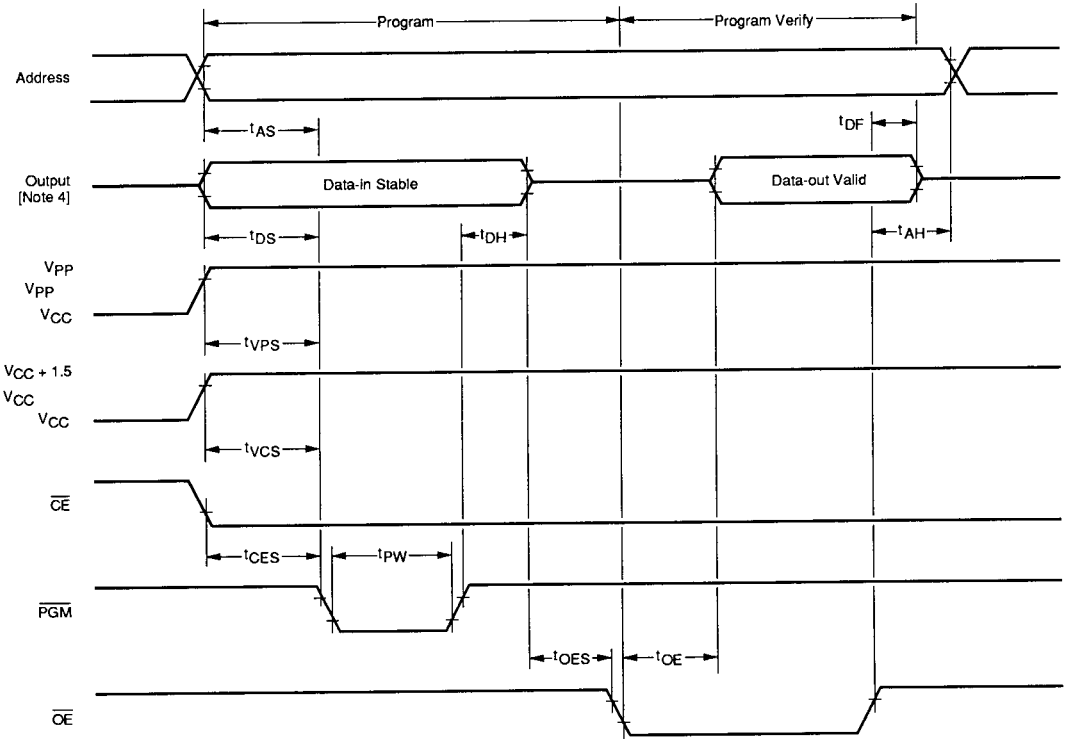
Timing Waveforms (cont)

Word Programming Cycle



Notes:

[1] V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

[2] V_{PP} must not be greater than +13.5 V, including overshoot.

[3] Removing and reinserting the device while a voltage of 12.5 V is applied to pin V_{PP} may affect device reliability.

[4] The output lines are also used for data input when programming the device.

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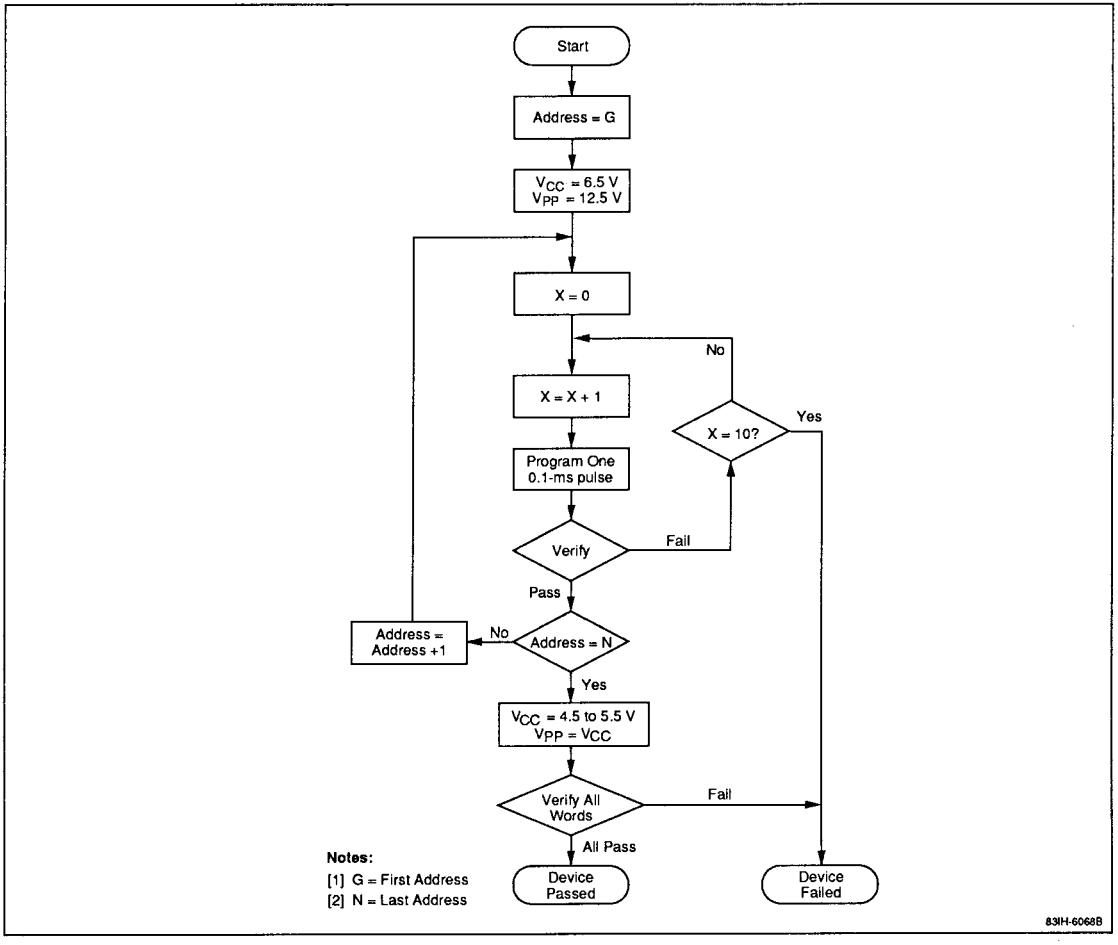
Figure 3 Word Programming Flowchart



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